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ANALYSIS OF VARIOUS CARRIER MODULATION SCHEMES FOR MODIFIED CHB MULTILEVEL INVERTER WITH HALF-BRIDGE CELL

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ABSTRACT

This paper comprises of various Carrier overlapping PWM scheme with performance evaluation for Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI). This topology consists of a Half Bridge cells DC voltage sources. Instead of 16-controlled switches used in conventional topology for 9-level output voltage, only twelve controlled switches are required for Modified Cascaded H-Bridge Multilevel Inverter topology which in turn reduces the complexity and also improves its performance parameters. The various carrier modulation schemes are applied to analyze its output voltage harmonics and $V_{rms.}$

INTRODUCTION

In recent years, the ongoing research in Multilevel Inverter is to further improve its capabilities, to optimize its control techniques and to minimize the device count and thereby reducing the manufacturing cost. Multilevel inverter concept is now incorporated over a wide range of high-power and medium power industrial applications which can be operated at high switching frequencies to produce lower order harmonic components (Franquelo *et al*., 2008). A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less EMI, and lower harmonic content (Du *et al*., 2006). The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources (Fang Zheng Peng, 2001). The cascaded H-bridge multilevel inverters (CHB-MLI) have found wide applications owing to the following advantages of the CHB-MLI first, due to modularity and the ability to operate at higher voltage levels. Second, the increased number of output voltage levels improves the quality of the inverter output voltage waveform which will be closer to a sinusoidal waveform (Leon *et al*., 2008). Moreover, high voltages can be managed at the dc and ac sides of the inverter, while each unit endures only a part of the total amount of dc voltage. The drawbacks of Cascaded H-Bridge inverters are i) Need for high number of semiconductor switches, ii) Involves separate DC for each H-bridge, iii) DC voltage balance control across all dc capacitors of the H-bridge units (Li and Wu, 2008). Furthermore, balancing unit's output fundamental voltages and minimizing harmonic distortion level still remain challenging issues (Rodriguez *et al*., 2002). A topology with reduction in number of switches used, will be considered as some form of enhancement in the plant on comparing with the traditional Cascaded H-Bridge inverters, for the same nine level output, in this Modified Cascaded H-Bridge multilevel inverter topology, the number of switches used reduces from 16 switches to 12 switches. Consequently

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this factor makes this Modified Cascaded H-Bridge multilevel inverter has value of significance. Hence this paper focuses on analysis and comparison of various parameters like THD & V_{rms} by applying various carrier modulation techniques.

Modified Cascaded H-bridge Multilevel Inverter Topology

General Structure

The general structure of the Modified cascaded multilevel inverter is shown in Fig. 1.

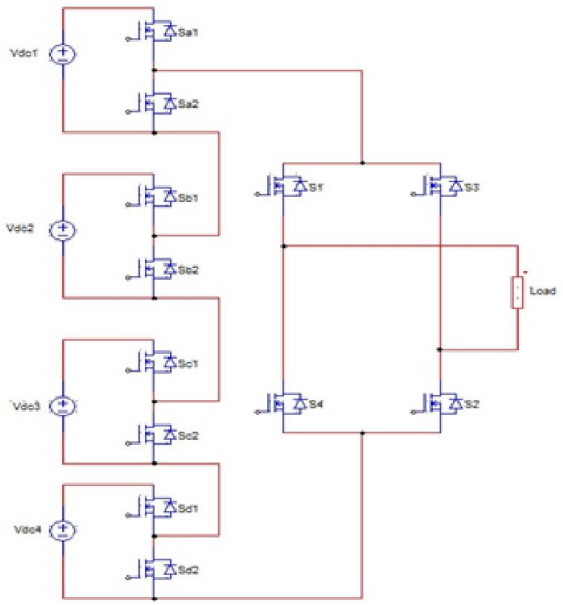

Figure 1. Modified-Cascaded multilevel inverter

Table 1. Switching Patterns for 9 levels Hybrid H-Bridge Multilevel Inverter

S. No	Half Bridge Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	Sa1,Sb1, Sc1, Sd1	Sa2,Sb2, Sc2, Sd2	S1, S2	S3, S4	$+4V_{dc}$
2	Sa2,Sb1, Sc1, Sd1	Sa1,Sb2, Sc2, Sd2	S1, S2	S3, S4	$+3V_{dc}$
3	Sa2,Sb2, Sc1, Sd1	Sa1,Sb1, Sc2, Sd2	S1, S2	S3, S4	$+2V_{dc}$
4	Sa2,Sb2, Sc2, Sd1	Sa1,Sb1, Sc1, Sd2	S1, S2	S3, S4	$+1V_{dc}$
5	Sa2,Sb2, Sc2, Sd2	Sa1,Sb1, Sc1, Sd1	S1, S3	S2, S4	0
6	Sa2,Sb2, Sc2, Sd1	Sa1,Sb1, Sc1, Sd2	S3, S4	S1, S2	$-1V_{dc}$
7	Sa2,Sb2, Sc1, Sd1	Sa1,Sb1, Sc2, Sd2	S3, S4	S1, S2	$-2V_{dc}$
8	Sa2,Sb1, Sc1, Sd1	Sa1,Sb2, Sc2, Sd2	S3, S4	S1, S2	$-3V_{dc}$
9	Sa1,Sb1, Sc1, Sd1	Sa2,Sb2, Sc2, Sd2	S3, S4	S1, S2	$-4V_{dc}$

The Modified Cascaded H-Bridge Multilevel Inverter proposed in this paper comprised of half-bridges and H-bridge inverters. The output of the cascaded half-bridges is the dc bus which is connected to the dc input of the H-bridge. Each half-bridge can make the DC source to be involved into the voltage producing or to be bypassed. By controlling the cascaded half-bridges, the number of DC sources connected in the circuit will be changed, that produces variable DC voltage. To produce ac waveforms, the H-bridge is just used to alternate the dc voltage direction. Hence, the full-bridge switching devices frequency is equal to the base frequency of the desired ac voltage.

Switching Operation

By turning on controlled switches S1, S2, (S3 and S4 turn off) the output voltage $+V_{dc}$ is produced across the load. Similarly turning on of switches S3, S4 (S1 & S2 turn off) V_{dc} output is produced across the load. Similarly turning on of switches S1, S3 (S2 & S4 turn off) Zero output is produced across the load. Table 1. clearly shows the switching patterns for 9 level of output voltage.

Multiple Carrier Pulse width Modulation Techniques

This paper emphases on applying carrier based PWM techniques to the M-CHB-MLI by using multiple carrier modulation schemes which has more than one carrier that can be triangular wave. The modulating / reference wave can be sinusoidal. For the particular reference wave, there is also multiple Control Freedom Degree including frequency, amplitude, phase angle of the reference wave. Similarly, carrier signal too have multiple Control Freedom Degree including frequency, amplitude, phase of each carrier and offsets between carriers. In these Multi carrier PWM schemes, several triangular carrier waves are compared with the single Sinusoidal reference wave. The number of carriers required to produce N level output is (m=n-1) where m is the number of carrier waveforms. The single sinusoidal reference waveform has peak to peak amplitude of A_m and a frequency f_m. The multiple triangular carrier waves are having same peak to peak amplitude A_c and frequency f_c (4). The single sinusoidal reference signal is continuously compared with all the carrier waveforms. A pulse is generated, whenever the single sinusoidal reference signal is greater than the carrier signal. The frequency ratio m_f is as follows

$$m_f = f_c / f_m$$

Though there are many carrier wave arrangements, in this paper, the following four arrangements have been carried out. THD and Vrms values for these four strategies for various modulation indexes are compared.

A. Carrier Overlapping Phase Disposition PWM strategy (CO-PD PWM).
B. Carrier Overlapping Phase Opposition Disposition PWM strategy (CO-POD PWM).
C. Carrier Overlapping Alternate Phase Opposition Disposition PWM strategy (CO-APOD PWM).
D. Variable Carrier Frequency PWM strategy (VCF-PWM).

Carrier Overlapping Phase Disposition PWM Scheme (CO-PD PWM)

The below Fig. 2 illustrates the Carrier overlapping PD PWM strategy (CO-PD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is A_c / 2. The reference waveform is centered in the middle of the carrier set. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching

device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for (CO-PD PWM) is

$$m_a = \frac{A_m}{(m/4)*A_c}$$

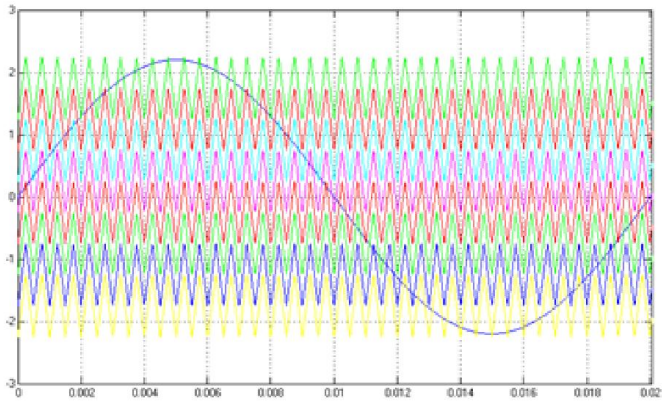

Fig.2. Carrier arrangement for Carrier Overlapping PD PWM strategy

Carrier Overlapping Phase Opposition Disposition PWM Scheme (CO-POD PWM)

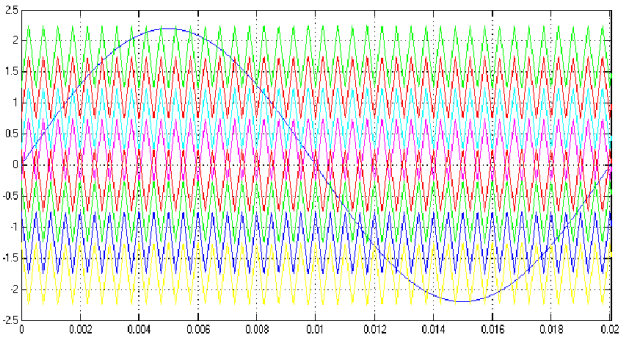

Fig.3. Carrier arrangement for Carrier Overlapping POD PWM strategy

The above Fig. 3 illustrates the Carrier overlapping POD PWM strategy (CO-POD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform is centered in the middle of the carrier set. The carrier waveforms above the zero reference are in phase. The carrier waveforms below are also in phase, but are 180 degrees phase shifted from those above zero. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for Carrier Overlapping Phase Opposition Disposition PWM Scheme (CO-POD PWM) is

$$m_a = \frac{A_m}{(m/4)*A_c}$$

Carrier Overlapping Alternate Phase Opposition Disposition PWM Scheme (CO-APOD-PWM)

The below Fig. 4 shows the Carrier Overlapping – APOD-PWM strategy (CO-APOD PWM), where the carriers with the same frequency f_c and same peak-to-peak amplitude A_c are phase displaced from each other by 180 degrees alternately and disposed such that the bands they occupy overlaps each other; the overlapping vertical distance between each carrier is $A_c/2$.

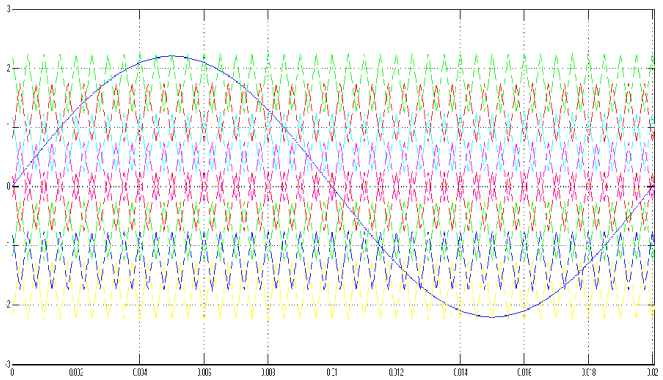

Fig. 4. Carrier arrangement for Carrier overlapping –APOD – PWM strategy

The reference waveform is centered in the middle of the carrier set. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. Amplitude modulation index for (CO-APOD PWM) is

$$m_a = \frac{A_m}{(m/4)*A_c}$$

Variable Carrier Frequency PWM strategy: (VCF-PWM)

The below Fig. 5 shows the Variable Carrier Frequency PWM strategy (VCF-PWM). For all PWM using constant frequency carriers, the number of switching operation for upper and lower devices of chosen multilevel inverter is much more than that of intermediate switches.

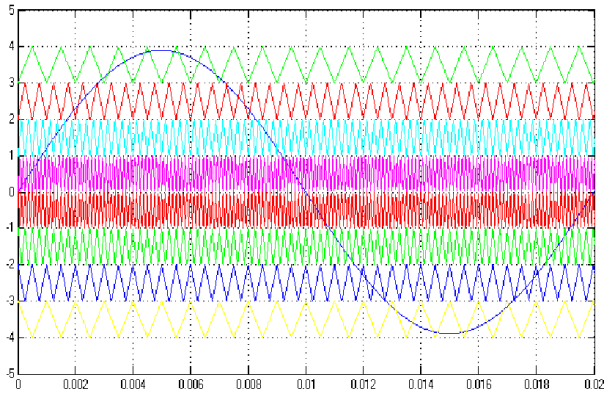

Fig. 5. Carrier arrangement for Variable Carrier Frequency PWM strategy

In order to equalize the number of switching operation for all the switches, variable frequency PWM strategy is used. The various carrier waveforms are in phase, but their frequencies are different. The carrier waveforms above and below the zero reference are in phase. The above Fig. 9 shows Complete Gate signal for 9-level M-CHB-MLI using VCF-PWM strategy. Amplitude Modulation index for the VCF-PWM is

$m_a = 2A_m / (m-1) A_c$

SIMULATION RESULTS

The Fig. 6 shown below is the simulink model of the Modified Cascaded H-Bridge Multilevel inverter (M-CHB-MLI). The following parameter values are used for simulation: V1 =100V, V2 =100V, V3 = 100V, V4= 100V, fc=2 KHz and fm=50 Hz. Gating signals for four different multi carrier strategies are simulated for 9-level M-CHB-MLI. Simulations are done for various values of M_a and the corresponding THD are observed using FFT block and listed in Table 2. The V_{rms} (fundamental) of the output voltage for various values of M_a and the corresponding Voltages are listed in Table 3.

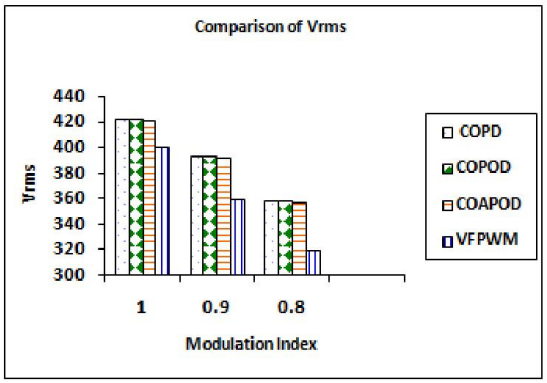

Fig. 7. Comparison of THD

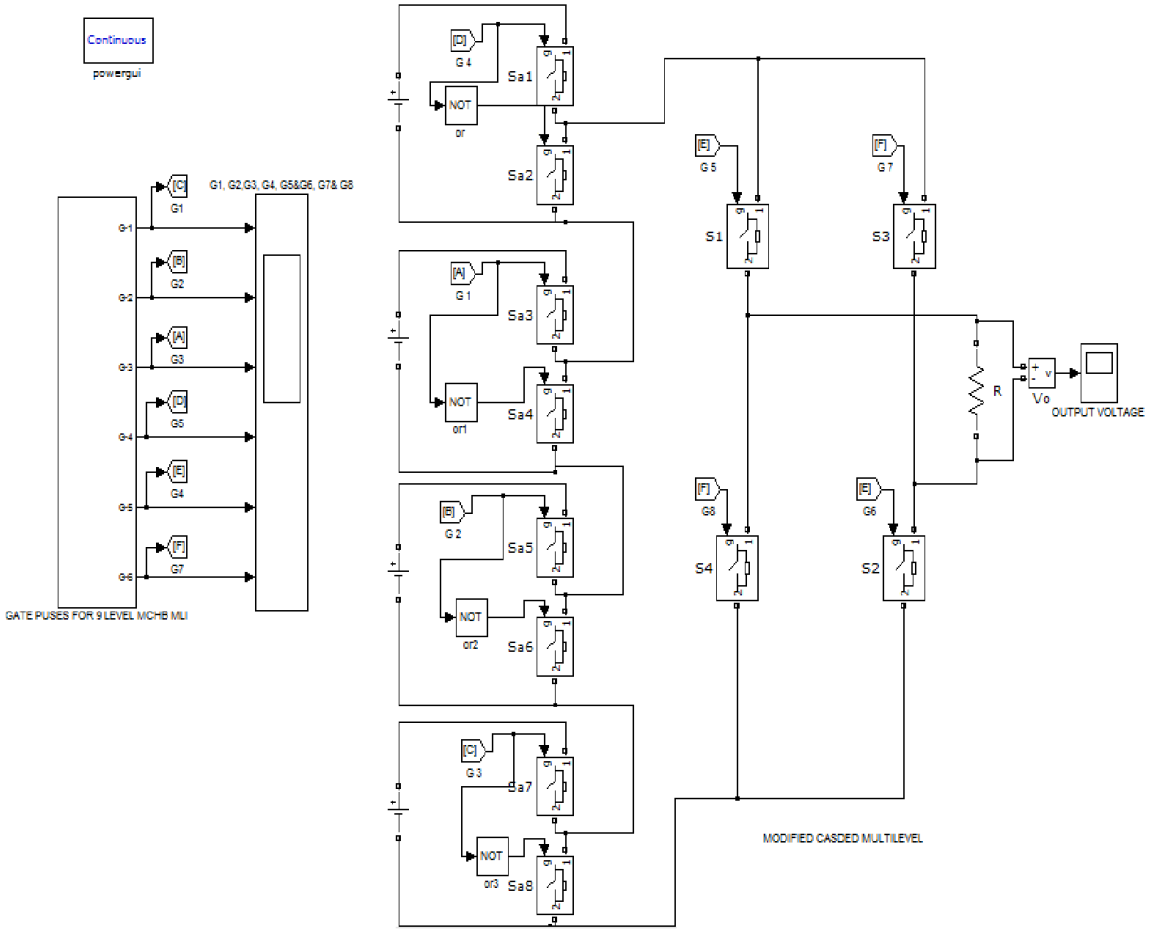

Fig. 6. Simulink Modeling of the Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI)

Table 2. Comparison of THD for various Multi carrier PWM Techniques

M_a	CO-PD PWM	CO-POD PWM	CO-APOD PWM	VCF-PWM
1	18.47	17.82	13.53	13.84
0.9	21.25	20.51	15.85	16.27
0.8	24.36	23.57	17.69	16.81

Table 3. Comparison of V_{rms} for various Multi carrier PWM Techniques

M_a	CO PD PWM	CO POD PWM	CO APOD PWM	VCF PWM
1	422.4	422.5	421.5	400.9
0.9	392.8	393	392.2	359.3
0.8	358.8	358.7	357.8	319.7

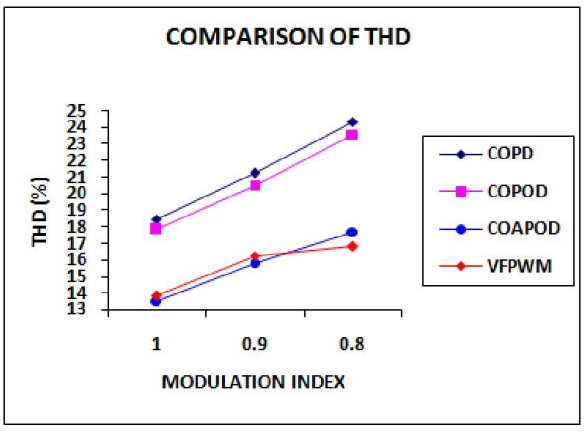

Fig. 8. Comparison of V_{rms}

The Simulated Output Voltage waveform of M-CHB-MLI using CO-PD PWM, CO-POD PWM, CO-APOD PWM and VCF-PWM Strategies are shown in the following Fig. 9 to Fig. 16. The Comparison of THD &V_{rms} for various Multicarrier PWM Techniques is shown in Fig 7 & 8.

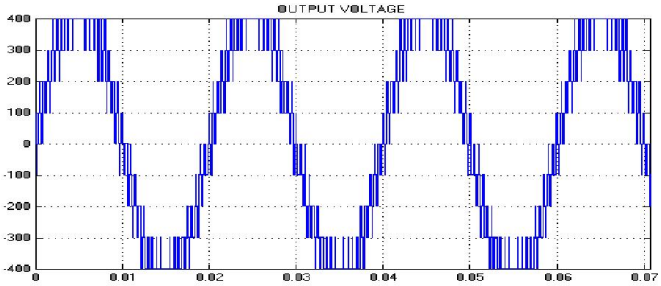

Fig. 9. Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-PD PWM Strategy

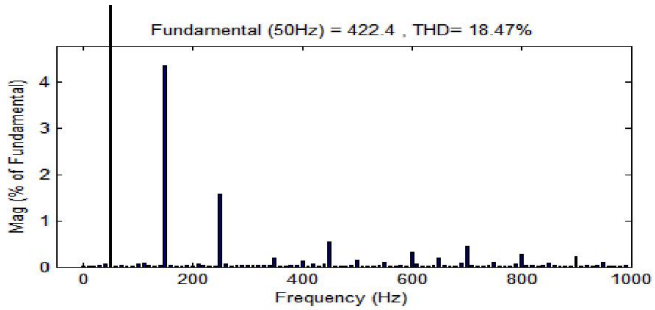

Fig. 10. FFT plot of 9-level M-CHB-MLI using CO-PD PWM strategy

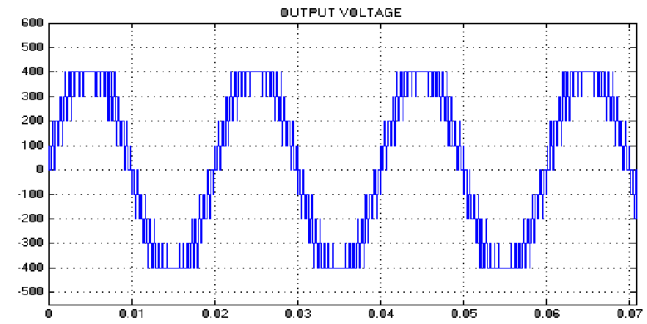

Fig. 11. Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-POD PWM Strategy

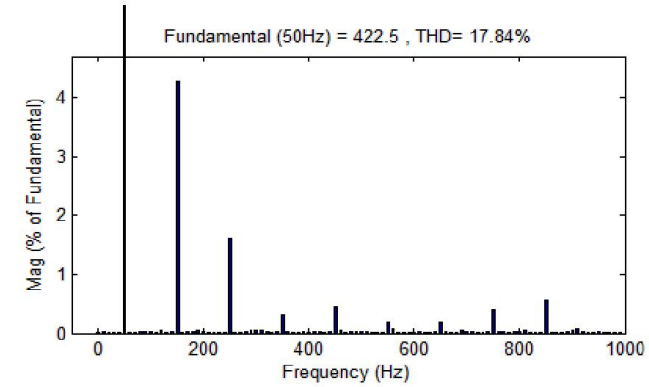

Fig. 12. FFT plot of 9-level M-CHB-MLI using CO-POD PWM Strategy

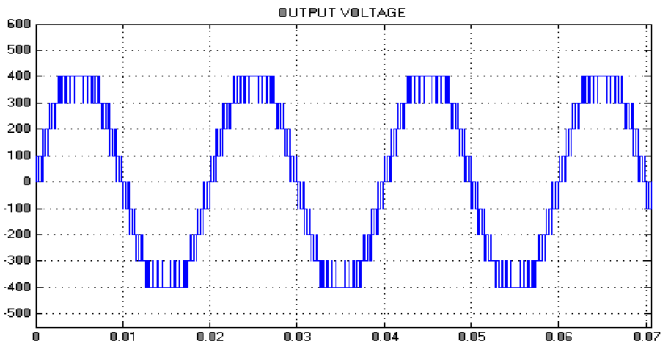

Fig. 13. Simulated 9-level Output Voltage waveform of M-CHB-MLI using CO-APOD PWM Strategy

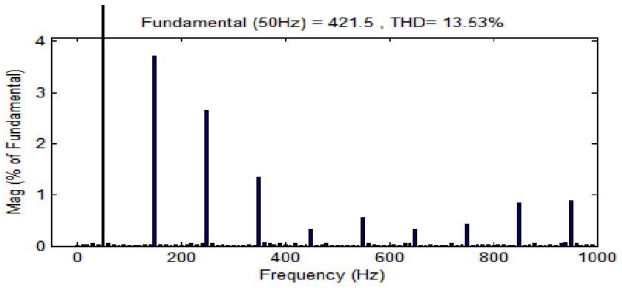

Fig. 14. FFT plot of 9-level M-CHB-MLI using CO-APOD PWM Strategy

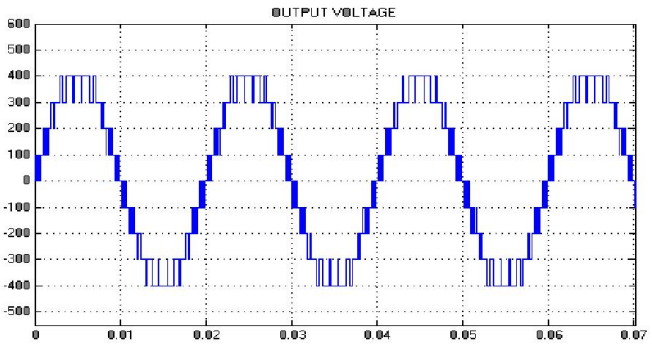

Fig. 15. Simulated 9-level Output Voltage waveform of M-CHB-MLI using VCF PWM Strategy

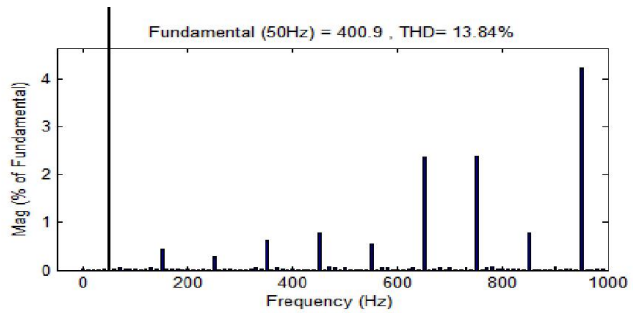

Fig. 16. FFT plot of 9-level MC-MLI using VCF PWM Strategy

Conclusion

In this paper, various Multi Carrier Modulation strategies for Single phase nine level Modified Cascaded H-Bridge Multilevel Inverter have been presented. Carrier wave overlapping technique have been applied to the Single phase nine levels Modified cascaded multilevel inverter and the

performance factors like THD and V_{RMS} have been analyzed and presented. It is inculcated that the Carrier overlapping Alternate Phase Opposition Disposition PWM strategy (CO-APOD-PWM) provides lower THD and higher V_{RMS} with less number of dominant harmonics than the other strategies. This nine level M-CHB-MLI engages only twelve switches, which eases cost and circuit complexity. Moreover it meritoriously diminishes lower order harmonics.

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